Unit 7 : A/D and D/A Converter

Lesson 1 : Interfacing with the Analog World

1.1. Learning Objectives

On completion of this lesson you will be able to :

- learn about various terms of A/D and D/A converters.

1.2. Interfacing with the Analog World

A digital quantity will have a value that is specified as one of two possibilities such as 0 or 1.

A digital quantity will have a value that is specified as one of two possibilities such as 0 or 1, LOW or HIGH, true or false, and so on. In practice, the voltage representation a digital quantity such as a may actually have a value that is anywhere within specified ranges. For example, for TTL logic :

0V to 0.8V = logic 0
2V to 5V = logic 1

Any voltage falling in the range 0 to 0.8 V is given the digital value 0, and any voltage in the range 2 to 5 V is assigned the digital value 1. The digital circuits respond accordingly to all voltage values within a given range.

Most physical variables are analog in nature and can take on any value within a continuous range of values.

Most physical variables are analog in nature and can take on any value within a continuous range of values. Examples include temperature, pressure, light intensity, audio signals, position, rotational speed, and flow rate. Digital systems perform all of their internal operations using digital circuitry and digital operations. Any information that has to be inputted to a digital system must first be put into digital form. Similarly, the outputs from a digital system are always in digital form.

1.2.1. Transducer

A transducer is a device that converts the physical variable to an electrical variable.

The physical variable is normally a nonelectrical quantity. A transducer is a device that converts the physical variable to an electrical variable. Some common transducers include thermistors, photocells, photodiodes, flow meters, pressure transducers, and tachometers. The electrical output of the transducer is an analog current or voltage that is proportional to the physical variable it is monitoring. For example, the physical variable could be the temperature of water. Let's say that the water temperature varies from 80 to 150^0 F and that a thermistor and its associated circuitry convert this water temperature to a voltage ranging from 800 to

1500mV. Note that the transducer's output is directly proportional to temperature; such that each 1^0 F produces a 10mV output. Analog-to-digital converter (ADC) and digital-to-converter (DAC) are used to interface a computer to the analog world so that the computer can monitor and control a physical variable Fig. 7.1.

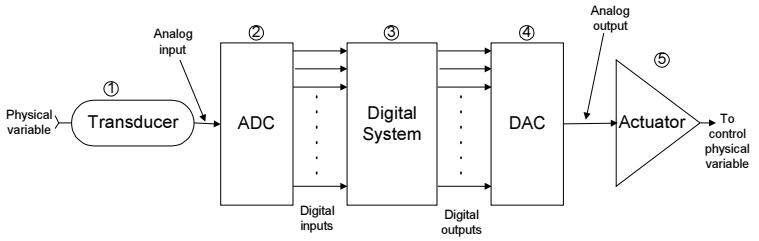

Fig. 7.1 : Interfacing with the analog world using Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC).

1.2.2. Analog-to-Digital Converter (ADC)

The transducer's electrical analog output serves as the analog input to the ADC. The ADC converts this analog input to a digital output.

The transducer's electrical analog output serves as the analog input to the ADC. The ADC converts this analog input to a digital output. This digital output consists of a number of bits that represent the value of the analog input. For example, the ADC might convert the transducer's 800- to 1500-mV analog values to binary values ranging from 01010000 (80) to 10010110 (150). Note that the binary output from the ADC is proportional to the analog input voltages so that each unit of the digital output represents 10mV.

The digital representation of the analog vales is transmitted from the ADC to the digital computer, which stores the digital value and processes it according to a program of instructions that it is executing.

1.2.3. Digital-to-Analog Converter (DAC)

This digital output from the computer is connected to a DAC, which converts it to a proportional analog voltage or current.

This digital output from the computer is connected to a DAC, which converts it to a proportional analog voltage or current. For example, the computer might produce a digital output ranging from 0000000 to 11111111, which the DAC converts to a voltage ranging from 0 to 10V.

1.2.4. Actuator

The analog signal from the DAC is often connected to some device or circuit that serves as an actuator to control the physical variable.

The analog signal from the DAC is often connected to some device or circuit that serves as an actuator to control the physical variable. For our water temperature example, the actuator might be an electrically controlled valve that regulates the flow of hot water into the tank in accordance with the analog voltage from the DAC. The flow rate would

vary in proportion to this analog voltage, with 0 V producing no flow and 10 V producing the maximum flow rate.

Thus we see that ADCs and DACs function as interfaces between a completely digital system, like a computer, and the analog world.

1.3. Digital-to-Analog Conversion

D/A conversion is the process of taking a value represented in digital code.

Basically, D/A conversion is the process of taking a value represented in digital code (such as straight binary or BCD) and converting it to a voltage or current which is proportional to the digital value. Fig. 7.2 shows the symbol for a typical 4-bit D/A converter. Now, we will examine the various input/output relationships.

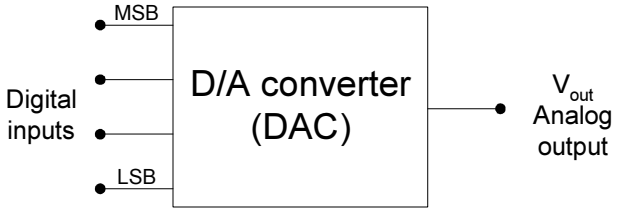

Fig. 7.2 : Four bit DAC with voltage output.

The digital inputs D,C,B, and A are usually derived from the output register of a digital system. The $2^4 = 16$ different binary numbers represented by these 4 bits for each input number, the D/A converter output voltage is a unique value. In fact, for this case, the analog output voltage Vout is equal in volts to the binary number.

In general,
Analog output = K × digital input

where K is the proportionality factor and it is constant value for a given DAC. The analog output can of course be a voltage or current. When it is a voltage, K will be in voltage units, and when the output is current, K will be in current units. For the DAC of K=1 V, so that

V_{OUT} = (1 V) × digital input

We can use this to calculate V_{OUT} for any value of digital input. For example, with a digital input of $1100_2 = 12_{10}$, we obtain

V_{OUT} = 1V × 12 = 12V

Problem 1

Problem 1 and Solution

A 5-bit DAC has a current output. For a digital input of 101000, an output current of 10mA is produced. What will IOUT be for a digital input of 11101?

Solution

The digital input 10100_2 is equal to decimal 20. Since I_{OUT} = 10 mA for this case, the proportionality factor as 0.5 mA. Thus, we can find for a digital input such as $11101_2 = 29_{10}$ as follows :

$I_{OUT} = (0.5mA) \times 29$
$= 14.5$ mA

Remember, the proportionality factor, K, will vary from one DAC to another.

Problem 2

What is the largest value of output voltage from an 8-bit DAC that produces 1.0V for a digital input of 00110010?

Solution

$00110010_2 = 50_{10}$
$1.0\ V = K \times 50$

Therefore,
$K = 20$ mV

The largest output will occur for an input of $11111111_2 = 255_{10}$.

$V_{OUT}(max) = 20mV \times 255$
$= 5.10$ V

Analog Output

Analog Output

The output of a DAC is technically not an analog quantity because it can take on only specific values like the 16 possible voltage levels for Vout. Thus, in that sense, it is actually digital. However, the number of different possible output levels can be increased and the difference between successive values can be decreased by increasing the number of input bits. This will allow us to produce an output that is more and more like an analog quantity that varies continuously over a range of values.

Input Weights

For the DAC of it should be noted that each digital input contributes a different amount to the analog output. This is easily seen if we examine the cases where only one input is HIGH Table 7.1. The contributions of each digital input are weighted according to their position in the binary number.

D	C	B	A		V_{OUT} (V)
0	0	0	1	→	1
0	0	1	0	→	2
0	1	0	0	→	4
1	0	0	0	→	8

Table 7.1

Thus, A, which is the LSB, has a weight of 1V, B has a weight of 2V, C has a weight of 4 V, and D, the MSB, has the largest weight 8V. The weights are successively doubled for each bit, beginning with the LSB. Thus, we can consider V_{OUT} to be the weighted sum of the digital inputs. For instance, to find V_{OUT} for the digital input 0111 we can add the weights of the C, B, and A bits to obtain 4 V + 2V + 1V=7V.

Problem 3

Input Weights Problem 3 and Solution

A 5-bit D/A converter produces V_{OUT} = 0.2 V for a digital input of 0001. Find the value of Vout for an input of 11111.

Solution

Obviously, 0.2 V is the weight of the LSB. Thus, the weights of the other bits must be 0.4 V, 0.8 V, 1.6 V, and 3.2 V respectively. For a digital input of 11111, then, the value of V_{OUT} will be 3.2 V + 1.6 V+ 0.8V + 0.4V + 0.2 V = 6.2 V.

1.4. Resolution

Resolution of a D/A converter is defined as the smallest change that can occur in he analog output as a result of a change in the digital input.

Resolution of a D/A converter is defined as the smallest change that can occur in he analog output as a result of a change in the digital input. We can see that the resolution is 1V, since V_{OUT} can change by no less than 1 V when the digital input value is changed. The resolution is always equal to the weight of the LSB and is also referred to as the step size. As the counter is being continually cycled through its 16 states by the clock signal, the DAC output is a staircase waveform that goes up 1 V per step. When the counter is at 1111, the DAC output is at its maximum value of 15 V; this is its full-scale output. When the counter recycles to

0000, the DAC output returns to 0V. The resolution or step size of the jumps in the staircase waveform; in this case, each step is 1 V.

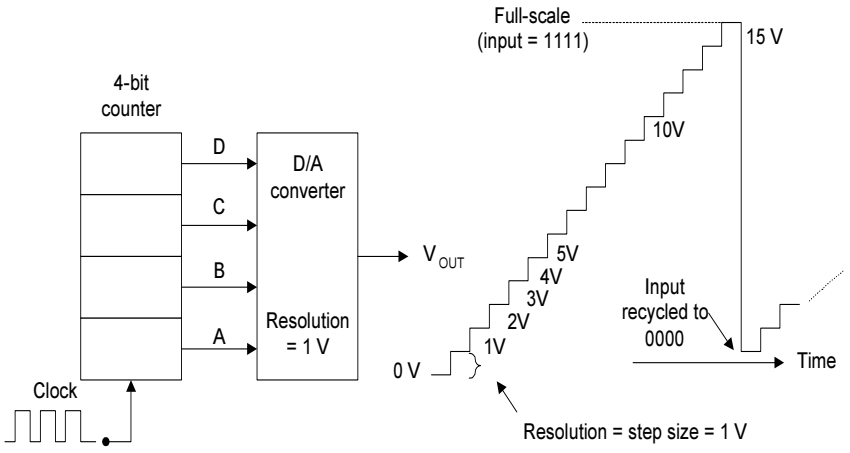

Fig. 7.3 : Output wave forms of a four bit DAC.

Note that the staircase has 16 levels corresponding to the 16 input states, but there are only 15 steps or jumps between the 0-V level and full-scale, In general, for an N-bit DAC the number of different levels will be 2^N, and the number of steps will be $2^N - 1$.

You may have already figured out the resolution (step size) is the same as the proportionality factor in the DAC input/output relationship :

$$\text{analog output} = K \times \text{digital input}$$

A new interpretation of this expression would be that the digital input is equal to the number of the step, K is the amount of voltage (or current) per step, and the analog output is the product of the two.

Problem 4

For the DAC of Example 3 determine V_{OUT} for a digital input of 10001.

Solution

The step size is 0.2 V, which is the proportionality factor K. The digital input is $10001 = 17_{10}$. Thus we have :

$V_{OUT} = (0.2\ V) \times 17$
$= 3.4V$

1.5. Percentage Resolution

Although resolution can be expressed as the amount of voltage or current per step, it is also useful to express it as a percentage of the full-scale output. To illustrate, in Fig. 7.3 the DAC has a maximum full-scale output of 15 V (when the digital input is 1111). The step size is 1V, which gives a percentage resolution.

$$\%\ resolution = \frac{step\ size}{full\ scale\ (F.S.)} \times 100\%$$
$$= \frac{1\,V}{15\,V} \times 100\% = 6.67\%$$

Percentage Resolution Problem 5 and Solution

Problem 5

A 10-bit DAC has a step size of 10 mV. Determine the full-scale output voltage and the percentage resolution.

Solution

With 10 bits, there will be 2^{10} - 1 = 1023 steps of 10mV each. The full-scale output will therefore be 10mV × 1023 = 10.23 V and

$$\%\ resolution = \frac{10\,mV}{10.23\,V} \times 100\% \approx 0.1\%$$

Problem 4 helps to illustrate the fact that the percentage resolution becomes smaller as the number of input bits is increased. In fact, the percentage resolution can also be calculated from.

$$\%\ resolution = \frac{1}{total\ number\ of\ steps} \times 100\%$$

For an N-bit binary input code the total number of steps is 2^N-1. Thus, for the previous example,

$$\%\ resolution = \frac{1}{2^{10} - 1} \times 100\%$$
$$= \frac{1}{1023} \times 100\%$$
$$\approx 0.1\%$$

This means that it is only the number of bits which determines the percentage resolution. Increase of the number of bits increases the number of steps to reach full scale.

1.6. Exercise

1.6.1. Multiple choice questions

a) Each digital input of DAC are weighted according to their position in the

i) binary number
ii) decimal number
iii) hexa- decimal number
iv) octal number.

b) The ADC converts analog input to a digital

i) input
ii) output
iii) number
iv) all of the above.

1.6.2. Questions for short answers

a) What is the function of a transducer and actuator?
b) What do you mean by input weights?
c) Define resolution. What is the full scale output?
d) What is the function of an ADC?
e) What function does a DAC perform?

1.6.3. Analytical question

a) “Five elements are involved when a computer is monitoring and controlling a physical variable that is assumed to be analog.” Illustrate the above situation.

Lesson 2 : D/A Converter

2.1. Learning Objectives

On completion of this lesson you will be able to :

- design different types of D/A converter circuit and describe their operation.
- understand the advantages, disadvantages, and limitation of several types of digital-to-analog converters (DAC).

2.2. D/A Converter

The purpose of a digital-to-analog converter is to convert a binary word to a proportional current or voltage.

The purpose of a digital-to-analog converter is to convert a binary word to a proportional current or voltage.

The binary weighted resistors produce binary-weighted current which are summed up by the op-amp to produce proportional output voltage. The binary word applied to the switches produces a proportional output voltage.

Several different binary codes such as straight binary, BCD and offset binary are commonly used as inputs to D/A converters.

2.2.1. D/A-Converter Circuitry

D/A-Converter Circuitry

There are several methods and circuits for producing the D/A operation. We shall examine several of the basic schemes, to gain an insight into the ideas used.

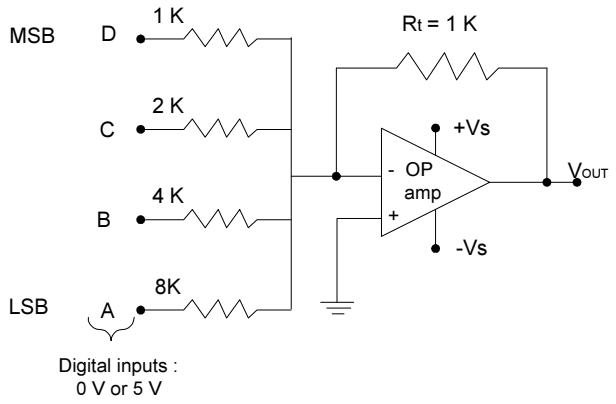

Fig. 7.4 : DAC circuitry using op-amp with binary weighted resistors.

Fig. 7.4 shows the basic circuit of 4-bit DAC. The inputs A,B,C, and D are binary inputs which are assumed to have values of either 0 V or 5 V. The operational amplifier is employed as a summing amplifier, which produces

the weighted sum of these input voltages. the summing amplifier multiplies each input voltage by the ratio of the feedback resistor R_F to the corresponding input resistor R_{IN}. In this circuit R_F R_{IN} 1kΩ and the input resistors range from 1 to 8 kΩ . The D input has R_{IN} = 1KΩ, so the summing amplifier passes the voltage at D with no attenuation. The C input has R_{IN} = 2 kΩ, so that it will be attenuated by. Similarly, the B input will be attenuated by ¼ and the A input by $^1/_8$. The amplifier output can thus be expressed as

$$V_{OUT} = - (V_D + {}^1/_2\ V_C + ¼\ V_B + {}^1/_8\ V_A)$$

The negative sign is present because the summing amplifier is a polarity-inverting amplifier, but it will but concern us here.

Clearly, the summing amplifier output is an analog voltage which represents a weighted sum of the digital inputs. The output is evaluated for any input condition by setting the appropriate inputs to either 0 V or 5 V. For example, if the digital input is 1010, then $V_D = V_B = 5V$ and $V_C = V_A = 0V$. Thus, using equation

$$\begin{aligned} V_{OUT} &= - (5V + OV + ¼ \times 5V + OV) \\ &= - 6.25V \end{aligned}$$

The resolution of this D/A converter is equal to the weighting of the lSB, which is $^1/_8 \times 5V = 0.625$ V. The analog output increases by 0.625 V as the binary input number advances one step.

Problem 6

Problem 6 Solution

Assume V_{REF} = 10 V and R = R = 10 kΩ. Determine the resolution and full-scale output for this DAC. Assume that R_L is much smaller than R.

Solution

$I_0 = V_{REE}/R = 1$ mA. This is the weight of the MSB. The other three currents will be 0.5, 0.25, and 0.125 mA. The LSB is 0.125 mA, which is also the resolution.

The full-scale output will occur when the binary inputs are all HIGH so that each current switch is closed and

$$I_{OUT} = 1 + 0.5 + 0.25 + 0.125 = 1.875 \text{ mA}$$

Note that the output current is proportional to V_{REF}. If V_{REF} is increased or decreased, the resolution and full-scale output will change proportionally.

2.3. R/2R Ladder

R/2R Ladder

The DAC circuits we have looked at, has some practical limitations. The biggest problem is the large difference in resistor values between the LSB and MSB, especially in high-resolution DACs. One of the most widely used DAC circuits that uses resistance's fairly close in value is the R/2R ladder network. Here the resistance values span a range of only 2 to 1.

Note, how the resistors are arranged, and only two different values are used, R and 2R. The current I_{OUT} depends on the positions of the four switches, and the binary inputs $B_3B_2B_1B_0$ control the states of the switches. This current is allowed to flow through an op-amp current-to-voltage converter to develop V_{OUT}. It can be shown that the value of V_{OUT} is given by the expression.

$$V_{OUT} = \frac{-V_{REF}}{8} \times B\,.$$

where B is the value of the binary input, which can range from 000 (0) to 1111 (15).

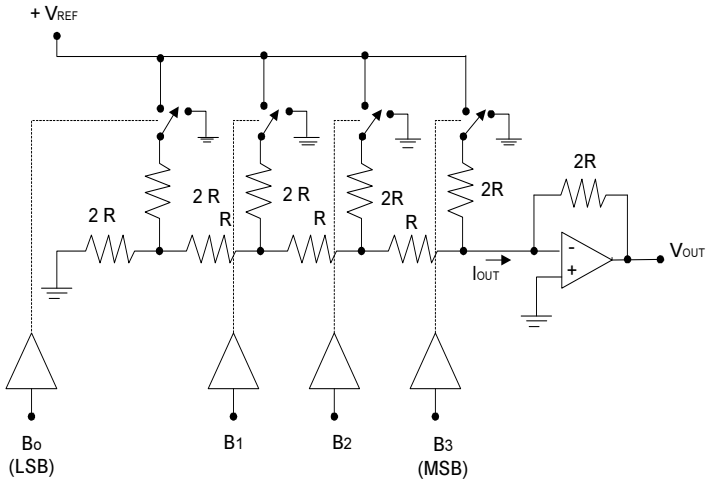

Fig. 7.5 : R/2R ladder DAC.

2.4. DAC Specifications

2.4.1. Resolution

Resolution
Accuracy

As mentioned earlier, the percentage resolution of a DAC is dependent on the number of bits. A 10-bit DAC has a finer (smaller) resolution than an 8-bit DAC.

2.4.2. Accuracy

There are several ways of specifying accuracy. The two most common are called full-scale error and linearity error. which are normally expressed as a percentage of the converter's full-scale output (%F.S.)

Full-scale error is the maximum deviation of the DAC's output from its expected (ideal) value, expressed as a percentage of full scale. For example, assume that the DCA has an accuracy of ± 0.01% F.S. Since this converter has a full-scale output of 9.375 V, this percentage converts to

$$\pm 0.01\% \times 9.375 \text{ V} = \pm 0.9375 \text{ mV}$$

This means that the output of this DAC can, at any time, be off by as much as 0.9375mV from its expected value.

Linearity error is the maximum deviation in step size from the ideal step size. For example, the DAC has an expected step size of 0.625 V. If this converter has a linearity error of ± 0.01F.S,, this would mean that the actual step size could be off by as much as 0.9375 mV.

Problem 7

Example 7 and Solution

A certain 8-bit DAC has a full-scale output of 2mA and a full-scale error of ± 0.5% F.S. What is the range of possible outputs for an input of 10000000?

Solution

The step size is 2mA/255 = 7.84 μA. Since 10000000 = 128_{10}, the ideal output should be 128 × 7.84 μA. The error can be as much as

$$\pm 0.5\% \times 2\text{mA} = \pm 10\mu\text{A}$$

Thus, the actual output can deviate by this amount from the ideal 1004μA , so the actual output can be anywhere from 994 to 1014 μA.

2.4.3. Offset Error

Offset Error

Ideally, the output of a DAC will be zero volts when the binary input is all 0's. In practice, however, there will be a very small output voltage for this situation; this is called offset error. This offset error, if not corrected, will be added to the expected DAC output for all input cases. Offset error can be negative as well as positive.

Many DACs will have an external offset adjustment that allows you to zero the offset. This is usually accomplished by applying all 0s to the DAC input and monitoring the output while an offset adjustment potentiometer is adjusted until the output is as close to 0 V as required.

2.4.4. Settling Time

Settling Time

The operating speed of a DAC is usually specified by giving its settling time, which is the time required for the DAC output to go from zero to full scale as the binary input is changed from all 0's to all 1's. Typical values for settling time range from 50 ns to 10 μs.

2.4.5. Monotonicity

A DAC is monotonic if its output increases as the binary input is incremented from one value to the next. Another way to describe this is that the staircase output will have no downward steps as the binary input is incremented from zero to full scale.

Monotonicity
DAC Applications
Control

2.5. DAC Applications

DACs are used whenever the output of a digital circuit has to provide an analog voltage or current to drive an analog device. Some of the most common applications are described in the following paragraphs.

2.5.1. Control

The digital output from a computer can be converted to an analog control signal to adjust the speed of a motor or the temperature of a furnace, to control almost any physical variable.

2.5.2. Automatic Testing

Automatic Testing
Signal Reconstruction

Computers can be programmed to generate the analog signals (through a DAC) needed to test analog circuitry. The test circuit's analog output response will normally be converted to a digital value by an ADC and fed into the computer to be stored, displayed, and sometimes analyzed.

2.5.3. Signal Reconstruction

In many applications, an analog signal is digitized, meaning that successive points on the signal are converted to their digital equivalent and stored in memory. This conversion is performed by an analog-to-digital converter (ADC). A DAC can then be used to convert the stored digitized data back to analog-one point at a time-thereby reconstructing the original signal. This combination of digitizing and reconstruction is

used in digital storage oscilloscopes, audio compact disk systems, and digital audio and video recording.

2.6. Exercise

2.6.1. Multiple choice questions

a) Resolution of DAC is equal to the weight of

i) LSB
ii) MSB
iii) full scale output
iv) 1 volt.

b) When the binary input is all 0.s, ideally the output of a DAC will be?

i) Zero volt
ii) Full scale output voltage
iii) 1 volt
iv) One step voltage.

2.6.2. Questions for short answers

a) Define full scale error and offset error.
b) What is the advantage of R/2R ladder DAC over the DAC that uses binary weighted resistors?
c) An 8-bit DAC has an output of 3.92 mA for an input of 01100010. What are the DAC's resolution and full-scale output?
d) What is the percentage resolution of an 8-bit DAC?
e) How many different output voltages can a 12-bit DAC produce?
f) Define full-scale error.
g) What is settling time?
h) Describe offset error and its effect on a DAC output.

2.6.3. Analytical questions

a) Describe the operation of a DAC.
b) What is the advantage of R/2R ladder DACs over those that use binary weighted resistors?
c) Discuss some of the DAC applications.

Lesson 3 : A/D Converter

3.1. Learning Objectives

On completion of this lesson you will be able to :

- understand the operation of various types of analog-to-digital converter circuitry such as the single ramp A/D, the digital ramp A/D circuit.
- compare the advantages and disadvantages of different analog-to-digital converter circuits

3.2. Analog-to-Digital Conversion

An analog-to-digital converter takes an analog input voltage and after a certain amount of time produces a digital output code which represents the analog input.

An analog-to-digital converter takes an analog input voltage and after a certain amount of time produces a digital output code which represents the analog input. The A/D conversion process is generally more complex and time-consuming than the D/A process. The techniques that are used provide and insight into what factors determine an ADCs performance.

Several important types of ADC utilize a DAC as part of their circuitry. Fig. 7.6 is a general block diagram for this class of ADC. The timing for the operation is provided by the input clock signal. The control unit contains the logic circuitry for generating the proper sequence of operations. The START COMMAND, initiates the conversion process, The op-amp compactor has two analog inputs and a digital output that switches states, depending on which analog input is greater.

The basic operation of ADC.

The basic operation of ADCs of this type consists of the following steps:

1. The START COMMAND pulse initiates the operation.
2. At a rate determined by the clock, the control unit continually modifies the binary number that is stored in the register.
3. The binary number in the register is converted to an analog voltage, V_{AX}, by the DAC.

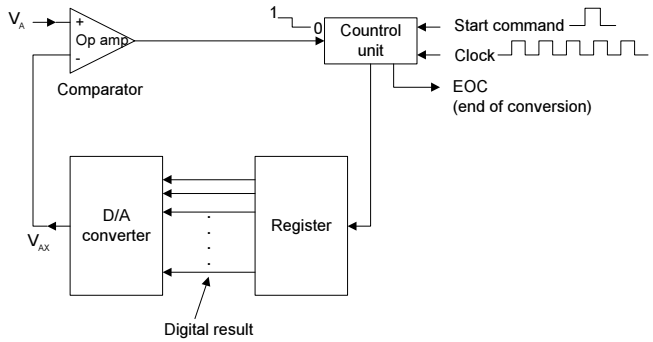

Fig. 7.6 : Basic diagram of ADC.

4. The comparator compares V_{AX} with the analog input V_A. As long as $V_{AX} < V_{A1}$ the comparator output stays HIGH. When V_{AX} exceeds V_A by at least an amount = V_T (threshold voltage), the comparator output goes LOW and stops the process of modifying the register number. At this point, V_{AX} is a close approximation to V_A. The digital number in the register, which is the digital equivalent of V_{AX}, is also the approximate digital equivalent of V_{A1} within the resolution and accuracy of the system.
5. The control logic activates the end-of-conversion signal, EOC, when the conversion is complete.

3.3. Digital-Ramp ADC

Operation procedure of a digital-ramp ADC.

One of the simplest versions of the general ADC of Fig. 7.7 uses a binary counter as the register and allows the clock to increment the counter one step at a time until $V_{AX} \geq V_A$. It is called a digital-ramp ADC because the wave form at V_{AX} is a step-by-step ramp (actually a staircase) like the one shown in Fig. 7.7. It is also referred to as a counter-type ADC. Fig. 7.7 is the diagram for a digital-ramp ADC. It contains a counter, a DAC, an analog comparator, and a control AND gate. The comparator output serves as the active-LOW end-of-conversion signal, $\overline{EOC}$. If we assume that V_A, the analog voltage to be converted, is positive, the operation proceeds as follows :

1. A START pulse is applied to reset the counter to zero. The HIGH at START also inhibits clock pulse form passing through the AND gate into the counter.
2. With all 0's at its input, the DAC's output will be $V_{AX} = 0V$.
3. Since $V_A > V_{AX}$, the comparator output, $\overline{EOC}$, will be HIGH.
4. When START returns LOW, the AND gate is enabled and clock pulses get through to the counter.
5. As the counter advances, the DAC output, V_{AX}, increases one step at a time as shown in Fig. 7.7.
6. This continues unit V_{AX} reaches a step that exceeds V_A by an amount equal to or greater than V_T (typically 10 to 100 μV). At this point, $\overline{EOC}$ will go LOW and inhibit the flow of pulses into the counter and the counter will stop counting.
7. The conversion process is now complete as signaled by the HIGH-to-LOW transition at $\overline{EOC}$, and the contents of the counter are the digital representation of V_A.
8. The counter will hold the digital value until the next START pulse initiates a new conversion.

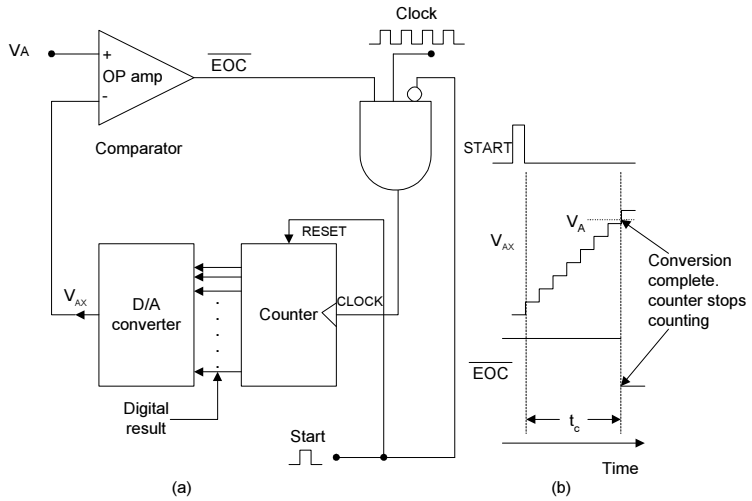

Fig. 7.7 : Digital-ramp ADC.

Problem 8

Assume the following values for the ADC clock frequency = 1 MHz; V_T = 0.1 mV; DAC has F.S. output = 10.23 V and a 10-bit input. Determine the following values.

Problem 8 and Solution

a. The digital equivalent obtained for V_A = 3.728 V.
b. The conversion time.
c. The resolution of this converter.

Solution

a. The DAC has a 10-bit input and a 10.23-V F.S. output. Thus, the number of total possible steps is 2^{10} - 1 = 1023, and so the step size is

$$\frac{10.23V}{1023} = 10mV$$

This means that V_{AX} increases in steps of 10 mV as the counter counts up from zero. Since V_A = 3.728 V and V_T = 0.1 mV, V_{AX} has to reach 3.7281 V or more before the comparator switches LOW. This will require.

$$\frac{3.7281V}{10mV} = 372.81 = 373\ steps$$

At the end of the conversion, then, the counter will bold the binary equivalent of 373, which is 0101110101. This is the desired digital equivalent of V_A = 3.728 V, as produced by this ADC.

b. Three hundred seventy-three steps were required to complete the conversion. Thus, 373 clock pulses occurred at the rate of one per microsecond. This gives a total conversion time of 373 μs.
c. The resolution of this converter is equal to step size of the DAC, which is 10mV. In percent it is $1/1023 \times 100\% \approx 0.1\%$.

Problem 9

Problem 9 and Solution

For the same ADC of problem 8 determine the approximate range of analog input voltages that will produce the same digital result of $0101110101_2 = 373_{10}$.

Solution

Table 7.2 shows the ideal DAC output voltage, V_{AX}, for several of the steps on and around the 373rd. If V_A is slightly smaller than 3.72 V (by an amount < V_T),

Step	V_{AX} (V)
371	3.71
372	3.72
373	3.73
374	3.74
375	3.75

Table 7.2

Then $\overline{EOC}$ won't go LOW when V_{AX} reaches the 3.72-V step, but will go LOW on the 3.73-V step. If V_A is slightly smaller than 3.73 V (by an amount < V_T), then $\overline{EOC}$ won't go LOW until V_{AX} reaches the 3.74-V step. Thus, as long as V_A is between approximately 3.72 V and 3.73-V, $\overline{EOC}$ will go LOW when V_{AX} reaches the 3.73-V step. The exact range of V_A values is

$$3.72 \text{ V} - V_T \text{ to } 3.73 \text{ V} - V_T$$

but since V_T is so small, we can simply say that the range is approximately 3.72 V to 3.73 V - a range equal to 10 mV, the DAC's resolution.

3.4. A/D Resolution and Accuracy

Resolution of the ADC is equal to the resolution of the DAC that it contains.

Resolution of the ADC is equal to the resolution of the DAC that it contains. The DAC output voltage V_{AX} is a staircase waveform that goes up in discrete steps until it exceeds V_A. Thus, V_{AX} is an approximation to the value of V_A, and the best we can expect is that V_{AX} is within 10 mV of V_A if the resolution (step size) is 10 mV. We can think of the resolution as being a built-in error that is often referred to as

quantization error. This quantization error, can be reduced by increasing the number of bits in the counter and DAC.

Problem 10

Problem 10 and Solution

Acertain 8-bit ADC hs a full-scale input of 2.55 V (i.e., V_A = 2.55 V produces a digital output of 11111111). It has a specified error of 0.1% F.S. Determine the maximum amount by which the V_{AX} output can differ from the analog input.

Solution

The step size is 2.55 V/ (2^8 - 1), which is exactly 10 mV. This means that even if the DAC has no inaccuracies, the V_{AX} output could be off by as much as 10 mV because V_{AX}. can change only in 10-mV steps; this is the quantization error. The specified error of 0.1% F.S. is 0.1% × 2.55 V = 2.55 mV. This means that the V_{AX} value can be off by as much as 2.55 mV because of component inaccuracies. Thus, the total possible error could be as much as 10 mV + 2.55 mV = 12.55 mV.

3.5. Conversion Time, TC

Conversion Time, TC

The conversion time is the time interval between the end of the START pulse and the activation of the $\overline{EOC}$ output. The counter starts counting from zero and counts up until V_{AX} exceeds V_A, at which point $\overline{EOC}$ goes LOW to end the conversion process. It should be clear that the value of conversion time, to, depends on V_A. A larger value will require more steps before the staircase voltage exceeds V_A.

The maximum conversion time will occur when V_A is just below full scale so that V_{AX} has to go to the last step to activate $\overline{EOC}$. For an N-bit converter this will be

$$\text{tc (max)} = 2^N - 1 \text{ clock cycles}$$

Sometimes, average conversion time is specified; it is half of the maximum conversion time.

$$tc(avg) = \frac{tc(\max)}{2} \approx 2^{N-1} \; clock \; cyles$$

The major disadvantage of the digital-ramp method is that conversion time essentially doubles for each bit that is added to the counter, so that resolution can be improved only at the cost of a longer tc. Applications,

however, the relative simplicity of the digital-ramp converter is an advantage over the more complex, higher-speed ADCs.

3.6. Applications

Applications

Almost any measurable quantity present as a voltage can be digitized by an A/D converter and displayed. A/D converters are the heart of digital voltmeters and digital MultiMate's. Analog voice signals are converted to digital form for transmission over long distances. At their destination they are reconverted to analog. In digital audio record- the analog audio signal produced by a microphone is digitized (using an ADC), then stored on some medium such as magnetic tope, magnetic disk or optical disk. Later the stored data are played back by sending them to a DAC to reconstruct the analog signal, which is fed to the amplifier and speaker system to produce the recorded sound.

3.7. Exercise

3.7.1. Multiple choice question

a) The number of total steps of a 9-bit ADC is,

i) 255
ii) 256
iii) 511
iv) 512.

3.7.2. Questions for short answers

a) What do you know about quantization error?
b) Define conversion time.
c) What is the major disadvantage of the digital ramp type ADC?
d) What is the function of the comparator in the ADC?
e) What is the function of the comparator in the ADC?
f) Where is the approximate digital equivalent of V_A when the conversion is complete?
g) What is the function of the $\overline{EOC}$ signal?

3.7.3. Analytical question

a) Draw digital ramp ADC and write down its operation.